REMARKS

This Amendment responds to the Office Action mailed February 23, 2006 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-14 are pending in the application. By this amendment, claims 1 and 8 have been amended. Accordingly, claims 1-14 are pending, with claims 1 and 11 being independent claims. No new matter has been added.

The Examiner has rejected claims 6, 7 and 9 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The Examiner asserts that the limitations of claims 6, 7 and 9 are not supported by the specification. The rejection is respectfully traversed.

The final paragraph on page 2 of the specification as filed makes it clear that the data items are always written to the same positions within the respective buffers, i.e., the "assigned specific addresses." Thus, claims 6 and 7 are supported by the specification. Regarding claim 9, it appears that the quoted paragraph of the specification at page 2, lines 16-22 may have been misread. The specification states that a transfer between the first and second buffers will be *allowed* when either *none or all* of the data items have been read by the processor. In other words and as recited in claim 9, the transfer of a group of temporally related items from the first buffer to the second buffer is *inhibited* if only *some* of the corresponding items in the second buffer have been read. For these reasons, it is submitted that claims 6, 7 and 9 are in full compliance with 35 U.S.C. §112, first paragraph, and withdrawal of the rejection is respectfully requested.

Claims 1-14 have been rejected under 35 U.S.C. §102(e) as anticipated by Patkar et al. (U.S. 6,449,671). The rejection is respectfully traversed.

Patkar discloses a method for efficiently allocating and operating cache memory in a multiprocessor computer system. Each processor is separately allocated primary cache and

second level cache depending on its operating requirements at the time (col. 3, lines 13-22). Read/write operations to the caches and external memory are controlled by a memory controller, which may also be responsible for determining the distribution of cache memory between the processors. The primary cache is operated in conventional manner in that it is filled by data from an external memory address specified by the processor along with a block of data from adjacent external memory addresses on the basis that one or more of these adjacent memory addresses will be subsequently required by the processor. Patkar states at col. 1, lines 42-43 that the data may be related temporally or spatially, but provides no explanation of this point.

Amended claim 1 is directed to a data transfer apparatus for controlling the provision of data to a data processor where the data comprises at least two data items having a predetermined temporal relationship to one another, the data items which are temporally associated with each other forming a group of data items. The apparatus includes a first buffer for receiving data from sources of data and including markers to indicate that a data item associated with the marker has been modified, and a data flow controller responsive to the markers and to a data association instruction specifying the data items which have a temporal relationship to one another and which form a group of data items such that the data flow controller only allows a group of data items having a predetermined temporal relationship to one another to be read from the first buffer when the items in the group satisfy the predetermined temporal relationship.

The invention is concerned with ensuring that multiple elements of data, such as sensor data, that have a temporal relationship are presented to a data processor as a complete set of information related to the same time frame so that they may be processed together. It prevents updating of elements of the related set of data with new data when the data processor has started a processing operation on the previous data set.

Claim 1 has been amended to clarify that the data comprises at least two data items having a predetermined temporal relationship to one another, the data items which are temporally associated with each other forming a group of data items. The data items identified by the

Examiner in Patkar, which are the individual data elements within a cache line, do not have a predetermined temporal relationship to one another and are, in fact, grouped together only as a result of the arbitrary selection of their contiguous cache addresses. The data elements within the cache line of Patkar are not temporally related, i.e., they do not relate to data taken from within the same time period, as is the case with the temporally related data of amended claim 1.

The Examiner cites the description of the Patkar system when transferring data from the primary to second level cache storage (Fig. 2 and col. 4, lines 8-52). When a block of data is no longer required by a first processor and is required to be written back to external memory, the memory controller attempts to move the block of data to second level cache by requesting whether a further processor, identified as having spare cache, can accept the data block. If the data is accepted, the memory controller transfers the data to the second level cache, freeing up the space in the first processor's primary cache. If the data cannot be accepted into the second level cache, the memory controller checks whether a "dirty bit" for the data block has been set. The dirty bit is set by the first processor if it has modified data at any of the addresses within the data block. If the dirty bit is set, the memory controller writes the data back to external memory. If the dirty bit is not set, this indicates that the cached data has not changed and the flush command from the first processor is ignored. It is noted that the dirty bit is set if any of the data within the block of addresses stored in the cache is changed and that there is no marker associated with individual addresses within the data block. In addition, the data is not associated with a fixed cache/buffer memory location either in the primary or second level caches.

It appears that the Examiner may have confused data having a temporal relationship with data stored temporarily. In the context of the present invention, data having a temporal relationship are data items that all relate to the same time period and have nothing to do with the length of time in which this data is held in corresponding buffers. In addition, the Examiner has not identified an element in Patkar that corresponds to the data association instruction recited by claim 1. In claim 1, the data association instruction specifies those data items that have a temporal relationship. In the embodiment described in the specification, the data association instruction is provided by the sensitivity register. No such data association instruction is

disclosed or suggested by Patkar. For at least these reasons, Patkar fails to disclose all the elements of claim 1. Accordingly, the rejection of claim 1 as anticipated by Patkar should be withdrawn.

Claims 2-10 depend from claim 1 and are patentable over Patkar for at least the same reasons as claim 1.

Claim 11 is directed to a method for controlling the provision of data to a processor wherein the data comprises a plurality of data items, at least two of which have a temporal relationship. Claim 11 contains method limitations that parallel the apparatus limitations of claim 11. Claim 11 is clearly and patentably distinguished over Patkar for at least the reasons discussed above in connection with claim 1. Claims 12-14 depend from claim 11 and are patentable over Patkar for at least the same reasons as claims 1 and 11.

Based upon the above discussion, claims 1-14 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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